

## METHOD AND APPARATUS FOR ENHANCED TIMING LOOP FOR A PRML DATA CHANNEL

### Abstract of the Disclosure

Methods and apparatus for enhanced timing loop are provided for a  
5 partial-response maximum-likelihood (PRML) data channel in a direct access  
storage device (DASD). An acquisition timing circuit for generating an  
acquisition timing signal includes a plurality of compare functions for  
receiving and comparing consecutive input signal samples on an interleave  
with a threshold value. The acquisition timing circuit includes a majority rule  
10 voting function coupled to the plurality of compare functions for selecting a  
timing interleave. Tracking timing circuitry for generating a timing error  
signal during a read operation includes a channel data detector. The  
channel data detector receives disk signal input samples and includes a  
multiple-state path memory. The tracking timing circuit includes a low  
15 latency detector receiving disk signal input samples. A selector function is  
coupled to an output of the low latency detector and is coupled to the  
multiple-state path memory for selecting a state. The selector function  
utilizes the low latency detector output and selects the state of the path  
memory. The selector function provides a low latency output corresponding  
20 to the selected state. The low latency output is used for generating the  
timing error signal during a read operation.